ABSTRACT

In a computer architecture using a prevalidated tag cache design, logic circuits are added to enable store and invalidation operations without impacting integer load data access times and to invalidate stale cache lines. The logic circuits may include a translation lookaside buffer (TLB) architecture to handle store operations in parallel with a smaller, faster integer load TLB architecture. A store valid module is added to the TLB architecture. The store valid module sets a valid bit when a new cache line is written. The valid bit is cleared on the occurrence of an invalidation operation. The valid bit prevents multiple store updates or invalidates for cache lines that are already invalid. In addition, an invalidation will block load hits on the cache line. A control logic is added to remove stale cache lines. When a cache line fill is being processed, the control logic determines if the cache line exists in any other cache segments. If the cache line exists, the control logic directs the clearing of store valid bits associated with the cache line.